IN THE CLAIMS

What is claimed is:

1. A non-volatile memory array, comprising:

a plurality of memory cells arranged in at least one row and at least one column, each memory cell including a drain region, a source region, a channel region disposed between the drain region and the source region, a floating gate disposed over at least the channel region, and a control gate disposed over the floating gate, the floating gate; and

at least one conductive member disposed along at least a portion of the row, said conductive member making contact with the sources of the memory cells of the portion of the row, said conductive member being self-aligned with the memory cells of said portion of the row.

2. The non-volatile memory array of claim 1, wherein:

said plurality of memory cells includes a first row of memory cells and a second row of memory cells adjacent to the first row, each of the memory cells along a portion of the first row sharing a common source with at least one memory cell of the second row; and

said conductive member is disposed along at least a portion of the first and second rows and makes contact with the common sources of the memory cells in said portion of the rows, the contact of said conductive member being self-aligned with the memory cells of said portion of the rows.

3. The non-volatile memory array of claim 1, wherein:

said plurality of memory cells includes a plurality of row pairs, at least a portion of the memory cells in each row pair having common source regions; and

a conductive member associated with each row pair, each conductive member being disposed along said portion of its respective row pair and making contact with the common sources thereof, the contact of each conductive member being self-aligned with the of the memory cells of said portion of its respective row pair.

4. The non-volatile memory array of claim 1, wherein:

said memory cells are arranged in a plurality of rows, the control gates of the memory cell in each row being commonly coupled to a word line extending generally parallel to the row; and

a conductive member associated with at least one row, each conductive member being disposed generally parallel to the word line along at least a portion of its respective row and making contact with the source regions thereof, the contact of each conductive member being self-aligned with the memory cells of said portion of its respective row.

5. The non-volatile memory array of claim 4, wherein:

each said conductive member overlaps the word line of its associated row along at least said portion of its respective row.

6. The non-volatile memory array of claim 4, wherein:

the plurality of rows includes pairs of adjacent rows, at least a portion of the memory cells of the pairs of adjacent rows sharing common source regions; and

each said conductive member is associated with a pair of adjacent rows, and is disposed generally parallel to the word lines of its respective pair of adjacent rows along at least a portion of pair of adjacent rows and makes contact with the common source regions thereof, each said conductive member overlapping the word lines of its associated pair of adjacent rows along at least said portion of its respective pair of adjacent rows.

7. The non-volatile memory array of claim 1, wherein:

said conductive member includes polysilicon.

8. The non-volatile memory array of claim 7, wherein:

said conductive member includes a metal silicide.

9. The non-volatile memory array of claim 7, wherein:

said conductive member includes a metal.

10. The non-volatile memory array of claim 1, including:

a plurality of conductive members; and

a source decoder and driving circuit for driving selected conductive members to an erase voltage in response to a plurality of source decode signals.

11. The non-volatile memory array of claim 10, including:

the plurality of source decode signals are generated in response to at least one memory address signal.

12. The non-volatile memory array of claim 10, including:

the plurality of source decode signals are generated in response to at least one user determined value.

13. In a flash erasable EPROM, a compact array, comprising:

a substrate;

a first flash erasable electrically programmable read-only memory (EPROM) cell formed on the substrate, and including a first cell top, a first cell first side, and a second cell second side opposite to the first cell first side;

a first cap insulator formed over the first cell top of said first flash EPROM cell;

a first insulating sidewall formed on the first side of the first flash EPROM cell; and

a conductive member disposed on at least a portion of said first insulating sidewall and making contact with a contact portion of the substrate adjacent to the first insulating sidewall.

14. The compact array of claim 13, wherein:

said first flash EPROM cell includes a first floating gate, a first interlayer dielectric and a first control gate formed over the first floating gate on the first interlayer dielectric.

15. The compact array of claim 13, wherein:

said conductive member includes a first layer of doped polysilicon.

16. The compact array of claim 13, wherein:

said conductive member includes a layer of metal silicide.

17. The compact array of claim 13, including:

a second flash EPROM cell formed adjacent to the first flash EPROM cell, the second flash EPROM cell including a second cell top, a second cell first side and second cell second side, the second cell second side opposing the first cell first side across the contact portion of the substrate;

a second cap insulator formed over the second cell top of said second flash EPROM cell;

a second insulating sidewall formed on the second side of the second flash EPROM cell; and

said conductive member is disposed on at least a portion of said second insulating sidewall.

18. The compact array of claim 17, wherein:

the contact portion of the substrate is a source region common to said first flash EPROM cell and said second flash EPROM cell.

19. The compact array of claim 13 wherein:

the contact portion of the substrate is a source region of said first flash EPROM cell.

20. In a flash EPROM memory device formed on a semiconductor substrate, an array configuration, comprising:

a plurality of flash EPROM cells arranged in an array having a plurality of rows extending in a row direction;

a plurality of source contacts formed along at least one row of the array, each said source contact being separated from an adjacent source contact by a substrate isolation region; and

a source connecting member extending in the row direction, disposed over, and making contact with, said plurality of source contacts.

21. The array configuration of claim 20, wherein:

said plurality of source contacts are formed along row pairs, each said source contact being shared by one flash EPROM cell of one row of the row pair and one flash EPROM cell of the other row of the row pair

22. The array configuration of claim 20, including:

a plurality of bit line contacts formed along at least one row of the array, opposite to said source contacts.

23. The array configuration of claim 20, including:

said source contacts are double diffused.

24. The array configuration of claim 20, including:

each flash EPROM cell includes a floating gate, the array further including a word line disposed along at least one of the rows, over and insulated from the floating gates of the row; and

and said plurality of contacts are self-aligned with the said word lines and the floating gates of the row.

25. The array configuration of claim 20, including:

a plurality of source connecting members; and

means for coupling a predetermined group of source connecting members to an erase voltage in response to a plurality of source decode signals.

26. The array configuration of claim 25, wherein:

said means for coupling includes

a plurality of source driver means for coupling at least one source connecting member to the erase voltage in response to driver input signal, and

a source decoder means for generating at least one driver input signal in response to the source decode signals.

27. The array configuration of claim 26, including:

address dependent source decode signal generating means responsive to a plurality of memory address signals for generating the source decode signals.

28. The array configuration of claim 26, including:

user dependent source decode signal generating means responsive to a plurality of predefined user values for generating the source decode signals.

29. The array configuration of claim 26, including:

configurable source decode signal generating means responsive to a plurality of predefined user values and memory address values for generating the source decode signals.